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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,985	09/22/2003	Yu-Jen Shen	251310-1090	1771

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,985	SHEN ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *8,17,30,39 and 43-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16,18-29,31-38 and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Embodiment 2, claims 1-7, 9-16, 18-29, 31-38, 40-42 and 52-53, in the reply filed on 11/08/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Embodiment 2, claims 1-7, 9-16, 18-29, 31-38, 40-42 and 52-53, in the reply filed on 11/08/04 is acknowledged. However, claims 52-53 are incomplete claims since they are depended on non-elected claim 45, therefore, claims 52-53 also be withdrawn.

Claims 8, 17, 30, 39, 43-51 and 54-56 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/08/04.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-16, 18-29, 31-38 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art of Figures 1A-1C in view of Yamashita (US 2002/0117756).

Applicants' Admitted Prior Art of Figures 1A-1C disclose a pad structure of semiconductor device, comprising:

a substrate (102);

an inter-layer dielectric (ILD) (106) layer formed over the substrate;

a first metallic layer (108) formed over the ILD;

a second metallic layer (114) formed over the first metallic layer, and a first inter-metal dielectric (IMD) layer (110) formed between the first metallic layer and the second metallic layer, wherein a plurality of first via holes (112) are formed in the first IMD layer;

a third metallic layer (120) formed over the second metallic layer, and a second inter-metal dielectric (IMD) layer (116) formed between the second metallic layer and the third metallic layer, wherein a plurality of second via holes (118) are formed in the second IMD layer. Applicants' Admitted Prior Art of Figures 1A-1C did not disclose the top surfaces of the second via holes compose a special via pattern, and the second IMD layer is divided into a plurality of separated (IMD) blocks by the second via holes. However, Yamashita discloses the top surfaces of the via holes (11m,22,31m) compose a special via pattern, and the IMD layer (10,20,30) is divided into a plurality of separated (IMD) blocks (11i,not shown,31i) by the via holes. Note Figures 4-6(f) of Yamashita. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top surfaces of the second via holes of Applicants' Admitted Prior Art of Figures 1A-1C composing a special via pattern and that the second IMD layer is divided into a plurality of separated (IMD) blocks by the second via holes, such as taught by Yamashita in order to prevent the occurrence of dishing in the conductive

portion. Note that it is inherent that the structure of Yamashita would reduce wire bonding cracks.

With regard to claim 2, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose an area proportion between the second via holes and the second IMD layer is larger than that between the first via holes and the first IMD layer.

With regard to claim 3, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the substrate is a silicon substrate.

With regard to claim 4, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the ILD layer is made of borophosphosilicate glass (BPSG).

With regard to claims 5 and 22, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose a field-oxide layer (104) is further interposed between the substrate and the ILD layer.

With regard to claims 6 and 23, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the first IMD layer and the second IMD layer are made of silicon oxide.

With regard to claims 7 and 24, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the first via holes and the second via holes are filled with tungsten (W).

With regard to claims 9-11, 18-20, 31-33 and 40-42, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita do not disclose the top surfaces of the second via holes or the special via pattern or both the first via pattern and the second via pattern are in a form of concentric frames, concentric circles, or spider web. However, it would have been obvious to one of ordinary skill in the art to form the via holes of Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita having the top surfaces being in a form as claimed, since it is well settled that, the change in shape of the top surfaces of the second via holes was a matter of design choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the trench was significant. *In re Dailey*, 357 F.2d 669, 149 USPTO 47 (CCPA 1996).

With regard to claim 12, 25 and 34-35, Applicants' Admitted Prior Art of Figures 1A-1C disclose a pad structure of semiconductor device, comprising:

a substrate (102);

an inter-layer dielectric (ILD) (106) layer formed over the substrate;

a first metallic layer (108) formed over the ILD;

a second metallic layer (114) formed over the first metallic layer, and a first inter-metal dielectric (IMD) layer (110) formed between the first metallic layer and the second metallic layer, wherein a plurality of first via holes (112) are formed in the first IMD layer;

a third metallic layer (120) formed over the second metallic layer, and a second inter-metal dielectric (IMD) layer (116) formed between the second metallic layer and the third metallic layer, wherein a plurality of second via holes (118) are formed in the second IMD layer.

Applicants' Admitted Prior Art of Figures 1A-1C did not disclose the first IMD layer is divided into a plurality of separated first IMD blocks by the first via holes, and the second IMD layer is divided into a plurality of separated second IMD blocks by the second via holes. However, Yamashita discloses the IMD layer (10,20,30) is divided into a plurality of separated IMD blocks (11i,not shown,31i) by the via holes (11m,22,31m). Note Figures 4-6(f) of Yamashita. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to divide the first and the second IMD layers of Applicants' Admitted Prior Art of Figures 1A-1C into a plurality of separated IMD blocks by the via holes, such as taught by Yamashita in order to prevent the occurrence of dishing in the conductive portion. Note that it is inherent that the structure of Yamashita would reduce or inhibit wire bonding cracks.

With regard to claims 13 and 36, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the second via holes are positioned above the first via holes. Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita do not disclose the second via holes are aligned with the first via holes. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second via holes of Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita being aligned with the first via holes in order to simplify the process by having the same pattern for forming the first and the second via holes.

With regard to claims 14 and 37, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the second via holes are positioned above and staggered from the first via holes.

With regard to claim 15, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose top surfaces of the first via holes compose a special first via pattern, and top surfaces of the second via holes compose a special second via pattern.

With regard to claims 16 and 38, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the first via pattern is identical with the second via pattern.

With regard to claim 21, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the substrate is a silicon substrate and the ILD layer is made of borophosphosilicate glass (BPSG).

With regard to claim 26, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose an area proportion between the via holes and the IMD layer with the separated IMD blocks is larger than that without the separated IMD blocks.

With regard to claim 27, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the ILD layer is made of borophosphosilicate glass (BPSG), and a field-oxide layer (104) is further interposed between the substrate and the ILD layer.

With regard to claim 28, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the IMD layers are made of silicon oxide, and the via holes are filled with tungsten (W).

With regard to claim 29, Applicants' Admitted Prior Art of Figures 1A-1C and Yamashita disclose the top surfaces of the via holes that separate the IMD layer into the IMD blocks compose a special via pattern.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

February 4, 2005

Hung Vu

Primary Examiner